CLAIMS

What is claimed is:

1. A DC canceler circuit comprising:
   a. a canceler input terminal adapted to receive a series of data input samples x(n);
   b. a canceler output terminal adapted to provide a series of data output samples y(n);
   c. a feedback path having:
      i. a feedback-path input terminal connected to the canceler output terminal;
      ii. a feedback-path output terminal connected to the canceler input terminal; and
      iii. a sigma-delta modulator having a sigma-delta input terminal connected to the feedback-path input terminal and a sigma-delta output terminal connected to the feedback-path output terminal.

2. The canceler circuit of claim 1, further comprising a subtractor having a first subtractor input node connected to the canceler input terminal and a second subtractor input node connected to the sigma-delta output terminal.

3. The canceler circuit of claim 1, further comprising a unit delay element having a delay-element input terminal connected to the feedback path input terminal and a delay-element output terminal connected to the sigma-delta input terminal.

4. The canceler circuit of claim 3, further comprising an adder having a first adder input terminal connected to the delay-element output terminal, a second adder input terminal connected to the feedback path input terminal, and an adder output terminal connected to the delay-element input terminal.

5. The canceler circuit of claim 4, wherein the adder connects to the feedback path input terminal via a multiplier.

6. A receiver comprising:
   a. a processing chip configured to include;
      i. a data input port;
      ii. a data output port;
      iii. sigma-delta modulator connected to the data input port and having a control-signal output port; and
   b. a feedback path connected between the control-signal output port and the data input port.

7. The receiver of claim 6, wherein the feedback path includes:
   a. an analog component having a filter input terminal; and
   b. an analog filter connected between the control-signal output port and the filter input terminal.

8. The receiver of claim 7, wherein the analog component includes an automatic gain control circuit.

9. The receiver of claim 7, wherein the analog component includes a voltage-controlled oscillator.

10. The receiver of claim 6, wherein the processing chip is programmable logic device.

11. The receiver of claim 10, wherein the programmable logic device is a field programmable gate array.

12. A sigma-delta loop having a tunable center frequency, the loop comprising:
    a. a data input terminal adapted to receive data x(n);
    b. a tunable all-pass network having an all-pass network input terminal connected to the data input terminal and an all-pass network output terminal;
    c. a global feedback network connected between the all-pass network output terminal and the all-pass network input terminal; and
    d. a local feedback network connected between the all-pass network output terminal and the all-pass network input terminal.

13. The sigma-delta loop of claim 12, further comprising a second tunable all-pass network having a second all-pass network input terminal, connected to the first-mentioned all-pass network output terminal, and a second all-pass network output terminal.

14. The sigma-delta loop of claim 12, wherein the global feedback network comprises:
    a. a first co-efficient multiplier connected between

the first-mentioned all-pass network output terminal and the first-mentioned all-pass network input terminal; and

b. a second co-efficient multiplier connected between the second all-pass network output terminal and the first-mentioned all-pass network input terminal.

15. The sigma-delta loop of claim 14, further comprising a quantizer having a quantizer input terminal connected to the global feedback network and a quantizer output terminal connected to the first-mentioned all-pass network input terminal.

16. A tunable sigma-delta loop comprising:

a. a data input terminal adapted to receive data x(n);

b. a first subtractor having a first input terminal, a second input terminal, and an output terminal;

c. a second subtractor having a first input terminal connected to the output terminal of the first subtractor, a second input terminal, and an output terminal;

d. a first adder having a first input terminal connected to the output terminal of the second adder, a second input terminal, and an output terminal;

e. a tunable all-pass network having an all-pass network input terminal connected to the output terminal of the first adder and an all-pass network output terminal connected to the second input terminal of the first adder;

f. a local feedback network having a local-feedback input terminal connected to the all-pass network output terminal and a local-feedback output terminal connected to the second input terminal of the of the second subtractor;

g. a global feedback network having a global-feedback input terminal connected to the all-pass network output terminal and a global-feedback output terminal; and

h. a quantizer having a quantizer input terminal connected to the global-feedback output terminal and a quantizer output terminal connected to the second input terminal of the first subtractor.

17. The loop of claim 16, further comprising:

a. a second adder having a first adder input terminal connected to the first-mentioned all-pass network output terminal, a second adder input terminal, and an adder output terminal connected to the local-feedback input terminal;

b. a second tunable all-pass network having an all-pass network input terminal connected to the output terminal of the second adder and a all-pass network output terminal connected to the second input terminal of the second adder;

c. a second global feedback network having a global-feedback input terminal connected to the all-pass network output terminal of the second all-bass network and a global-feedback output terminal;

d. a third adder having a first input terminal connected to the global-feedback output terminal of the first-mentioned global feedback network, a

second input terminal connected to the global-feedback output terminal of the second global feedback network, and an output terminal connected to the quantizer input terminal.